Analysis of RF Performances of GaN MESFETs Including Self-Heating and Trapping Effects

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Abstract — **A physics-based large-signal model of GaN-MESFET is reported which includes temperature dependences of transport and trapping parameters. RF power performances are analyzed using generalized Volterra series technique. At 2GHz, calculated maximum output power of a 0.3μm × 100μm GaN MESFET is 22.8dBm at the power gain of 6.1dB and power added efficiency of 28.5%. The corresponding quantities are in excellent agreement with the measured values of 23dBm, 5.8dB and 27.5%, respectively. At 2GHz, gain compressions due to self-heating effect of 2.2dB and 0.75dB are obtained for 0.30μm × 100μm and 0.75μm × 100μm GaN MESFETs, respectively. At 4GHz and 10dBm output power, calculated third-order intermodulations (IM3) for 0.30μm × 100μm and 0.75μm × 100μm GaN MESFETs are -56dBc and -44dBc, respectively. For the same devices, IM3 increases by 6dBc and 3dBc due to self-heating effects, respectively.**

I. Introduction

In recent years, GaN-based devices have received increased attention for wide variety of high power, high frequency and high temperature applications. The high peak and saturation velocity as well as low parasitic have resulted GaN based devices with f_T = 107GHz (0.15μm × 100μm GaN/$Al_{0.20}Ga_{0.80}N$ HEMT) [1] and f_{max} = 155GHz (0.12μm × 100μm GaN/$Al_{0.20}Ga_{0.80}N$ HEMT) [2]. Unique material properties of GaN such as high thermal conductivity and breakdown voltage have enabled these devices to be operated up to 11.8 W/mm at 10GHz using 0.3μm × 100μm AlGaN/GaN HEMT [3]. Power amplifiers using GaN HEMTs with output powers 14W at 8GHz [4] and 36W at 2.2GHz [5] have been demonstrated. However, GaN-based devices operating at high power density suffer from self-heating effects [6-8]. Using Raman spectroscopy Kuball *et al.* [6] estimated the temperature at the gate-drain opening to be 180C for a 4μm × 200μm GaN HFET grown on Sapphire at drain and gate bias of 20V and 0V, respectively. For the same bias voltages the temperature increase was 120C for a 1μm × 200μm GaN HFET grown on SiC. For a 250μm width GaN HFET grown on SiC, maximum temperature of 96C was reported in the active channel with a continuous wave dissipation power density of 5W/mm [7]. With Sapphire as substrate, the maximum temperature as high as 300C has been reported [7]. Using DC-*IV* measurements, a decrease of maximum power dissipation capability from 5.5W at 150K to 1.67W at 293K for the same device grown on SiC has been reported [7]. Nuttinck *et al.* [8] reported about 25% reduction in drain current as the drain pulse width increased from 1% to 100% at 300K for the 250μm width GaN HFET grown on SiC. The gate bias and peak drain voltage were 0V and 35V, respectively.

The self-heating effects at large drain bias increase the device lattice temperature and reduce the physical parameters such as mobility and carrier saturation velocity by increasing the carrier phonon scattering. As a result, device parameters such as, transconductance and output resistance become dependent on temperature and applied electric field [9-10]. Besides, GaN based devices are plagued by traps which results in current collapse in the *I-V* characteristics and DC to RF dispersion of transconductance and output resistance. The recovery of current collapse depends on the detrapping time constant which determines the dispersion frequency of the transconductance and output resistance. The dispersion frequency due to shallow traps in GaN increases exponentially with increasing temperature and can be of the order MHz at 600K [11]. Therefore, an exact analysis of GaN based devices should incorporate a thermal simulator to calculate operating temperature and corresponding physical and trapping parameters.

In this paper, an exact simulation technique to calculate RF power performances of GaN-based MESFETs considering thermal and trapping effects is reported. Junction temperature is calculated by solving Laplace's equation. The temperature and electric field dependences of transport parameters are obtained by using an ensemble Monte Carlo simulation. Model parameters are calculated by using a physics-based analysis and RF power performances are determined by using Volterra series analysis [11].

II. Analysis

At high electric field, velocity saturation occurs and mobility becomes electric field dependent. Besides,

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saturation velocity decreases with increasing temperature [9-10] and forces the mobility to be temperature dependent. Carrier velocity-electric field characteristic can be expressed as: $v(E,T)=\mu_{n0}(T)E/[1+E/E_{cr}(T)]$, where v is the electron velocity, E is the electric field, T is the absolute temperature, E_{cr} is the critical electric field which is given by $E_{cr}(T)=v_{sat}(T)/\mu_{n0}(T)$, v_{sat} is the saturation electron velocity and μ_{n0} is the low-field mobility. Mobility at a given temperature and electric field is given by, $\mu_n(E,T)=v(E,T)/E$. In the prescnt analysis, the temperature and electric field dependences of mobility and temperature dependence of saturation velocity and critical electrical field are expressed as:

$$\mu_n(E,T)=\sum_{i=0}^{2}\left(\sum_{j=0}^{2}k_{\mu ij}E^j\right)T^i, \qquad (1)$$

$$v_{sat}(T)=\sum_{m=0}^{2}k_{vm}T^m \text{ and } E_{cr}(T)=\sum_{n=0}^{2}k_{Ecrn}T^n \quad (2,3)$$

where $k_{\mu ij}$, k_{vm} and k_{Ecrn} are constants obtained by an ensemble Monte Carlo simulation [9-10]. $k_{\mu ij}$ are given in Table I. With v_{sat} in cm/s, E_{cr} in kV/cm and T in K, k_{vm} and k_{Ecrn} are estimated as: $k_{v0}=2\times10^7$, $k_{v1}=5000$, $k_{v2}=-25$, $k_{Ecr0}=145.25$, $k_{Ecr1}=-0.025$ and $k_{Ecr2}=0.0001$ [9].

Fig.1 shows the circuit model to include the effects of carrier trapping on frequency dispersion of output resistance and transconductance. The effects of traps are incorporated through the parameters C_{ss}, $g_m^{''}$ and $R_{ds}^{''}$ which are obtained based on the physical processes governing trap dynamics [11-12]. Intrinsic circuit parameters: C_{gs}, C_{gd}, $g_m^{'}$, R_i and $R_{ds}^{'}$ are obtained incorporating velocity saturation effects and temperature dependences transport parameters. In the saturation mode of operation the channel can be divided into linear or field dependent mobility region (length = L_1) and saturation velocity region (length = $L - L_1$). The intrinsic transconductance and output resistance given in Eqs. (4) and (5) are then obtained from the I-V relationship. Here, n_i is the intrinsic carrier concentration, ε is the GaN dielectric constant, q is the electronic charge, k is the Boltzmann constant, μ_n is the electron mobility at temperature T and electric field E, d is the thickness of the channel, W is the width of the device, L is the gate length, γ is the saturation factor, N_d is the channel doping concentration, $u_d=\sqrt{(V_{bi}+V_{DS}-V_{GS})/V_{pi}}$,

$u_0=\sqrt{(V_{bi}-V_{GS})/V_{pi}}$, $u_1=\sqrt{(V_{bi}+V(L_1)-V_{GS})/V_{pi}}$,

$V_{DS,sat}=V_{pi}(u_s^2-u_0^2)$, $V_{bi}=(kT/q)\ln(N_d/n_i)$,

$V_{pi}=qN_dd^2/2\varepsilon$, $C_{11}=\mu_n(E,T)(1-u_0)/\gamma v_{sat}(T)(1-u_1)$,

$C_{12}=L_1/(1-u_1)+qN_dd^2\mu_n(E,T)u_1/\varepsilon\gamma v_{sat}(T)$,

$C_{21}=\dfrac{qN_dd^2}{6\varepsilon\gamma v_{sat}(T)(1-u_1)}\left[3(u_1^2-u_0^2)-2(u_1^3-u_0^3)\right]\dfrac{\partial\mu_n(E,T)}{\partial V_{DS}}$,

and $C_{22}=C_{12}$. L_1 and u_1 are calculated by simultaneously solving,

$$L_1=\frac{qN_dd^2\mu_n(E,T)}{6\varepsilon\gamma v_{sat}(1-u_1)}\left[3(u_1^2-u_0^2)-2(u_1^3-u_0^3)\right] \text{ and}$$

$$V_{pi}(u_1^2-u_0^2)+\frac{2E_{cr}(T)du_1}{\pi}\sinh\left[\frac{\pi(L-L_1)}{2du_1}\right]=V_{DS},$$

which are obtained by equating drain currents at L_1 and solving Poission's equation in the depletion region. Capacitances C_{gs} and C_{gd} are obtained by assuming abrupt junction and intrinsic resistance R_i is given by,

$$g_m^{'}=\left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}=\begin{cases}-\dfrac{W}{L}qN_d\mu_n(E,T)d(u_d-u_0), & V_{DS}\le V_{DS,sat}\\[2ex] -\dfrac{qN_dv_{sat}(T)\gamma Wd\left\{1-C_{11}E_{cr}(T)\cosh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]\right\}}{2u_1V_{pi}+\dfrac{2E_{cr}(T)d}{\pi}\sinh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]-E_{cr}\left(C_{12}+\dfrac{L-L_1}{u_1}\right)\cosh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]}, & V_{DS}\ge V_{DS,sat}\end{cases} \qquad (4)$$

$$R_{ds}^{'}=\frac{1}{\left.\dfrac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}}}=\begin{cases}\dfrac{1}{\dfrac{q^2N_d^2Wd^3}{6\varepsilon L}\left\{\dfrac{3\mu_n(E,T)(1-u_d)}{V_{pi}}+\left[3(u_d^2-u_0^2)-2(u_d^3-u_0^3)\right]\dfrac{\partial\mu_n(E,T)}{\partial V_{DS}}\right\}}, & V_{DS}\le V_{DS,sat}\\[2ex] \left[\dfrac{qN_dv_{sat}(T)\gamma Wd\left\{1+C_{21}E_{cr}(T)\cosh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]\right\}}{2u_1V_{pi}+\dfrac{2E_{cr}(T)d}{\pi}\sinh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]-E_{cr}\left(C_{22}+\dfrac{L-L_1}{u_1}\right)\cosh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]}\right]^{-1}, & V_{DS}\ge V_{DS,sat}\end{cases} \qquad (5)$$

TABLE I

MOBILITY COEFFICIENTS OF EQ. (1) (μ - cm^2/v.s, T - K AND E - kV/cm)

L	$k_{\mu 00}$	$k_{\mu 01}$	$k_{\mu 02}$	$k_{\mu 10}$	$k_{\mu 11}$	$k_{\mu 12}$	$k_{\mu 20}$	$K_{\mu 21}$	$k_{\mu 22}$
1.50μm	2073.5	–40.15	0.2074	–4.7459	0.1076	–0.0006	0.0043	-1×10^{-4}	6×10^{-7}
0.75μm	1914.4	–36.18	0.1855	–4.3000	0.0900	–0.00053	0.0032	-8×10^{-5}	5×10^{-7}
0.50μm	1764.7	–32.43	0.1646	–3.8321	0.0856	–0.0005	0.0021	-6×10^{-5}	3×10^{-7}
0.30μm	1705.2	–30.91	0.1564	–3.3531	0.0750	–0.0004	0.0015	-4×10^{-5}	2×10^{-7}
0.10μm	1645.8	–29.40	0.1482	–2.8740	0.0644	–0.0003	0.0010	-3×10^{-5}	2×10^{-7}

$R_i \approx 1/\eta g_m'$ where,

$\eta \approx 2\left[1+2\beta L_1/3(1-\beta)(L+L_{gd})\right]^2$,

$\beta \approx 1/\sqrt{1+2(V_{GS}-V_{OFF})\mu_n(E,T)/Lv_{sat}(T)}$, L_{gd} is the gate-drain separation and V_{OFF} is the turn-off voltage [12]. The 0.3μm×100μm GaN MESFET reported by Gaquiere *et al.* [13] is used for simulation in this paper. The device has an active layer thickness, d = 200nm, channel doping concentration, N_d = 2.7 × 10^{17}cm^{-3} and source-drain separation, L_{sd} = 2.3μm. Using N_{to} = 1×10^{16} cm^{-3}, the constants of V_{DS}^{ONSET} are estimated as: a_0 = 4.15V, a_1 = 0.66, a_2 = 0.005V^{-1} and α = 0.0873V^{-1} [11]. The turn-off voltage V_{OFF} is estimated to be –8V. The other circuit parameters are obtained from reported experimental data and are as follows: R_g = 6 Ω, L_g = 0.055 nH, R_d = 70 Ω, L_d = 0.307 nH, R_s = 90 Ω, L_s = 0.027 nH and C_{ds} = 0.040 pF [11].

A thermal simulator is incorporated in the analysis to calculate the junction temperature by solving Laplace's equation for a given power dissipation. The analysis proceeds with the initial guess of junction temperature to estimate mobility, carrier velocity and critical electric field for a given channel electric field. Estimated mobility, carrier velocity and critical electric field are then used to compute drain current. The calculation is repeated until consistent solution for drain current, mobility, carrier velocity, critical electric field and temperature are obtained. The detrapping time constant and the dispersion frequency are calculated at the channel temperature. The model parameters are then calculated and output power, power gain and intermodulation for a given input power are obtained by using Volterra series analysis [11].

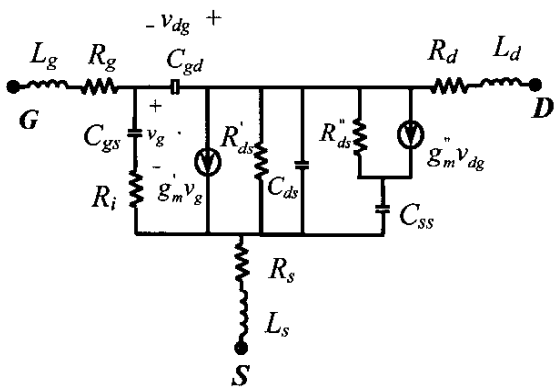

Fig. 1. GaN MESFET large signal model.

III. RESULTS AND DISCUSSION

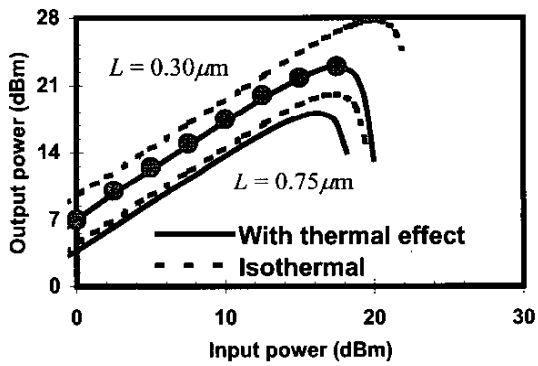

Fig. 2. Variation of output power as a function of input power for L×100μm GaN MESFET at 2GHz. Measured results are shown by circles for L = 0.3μm [13].

Fig.2 shows the variation of output power as a function of input power with gate length as a parameter at 2GHz. The bias voltages are V_{GS} = -2V and V_{DS} = 30V. Measured data for L = 0.3μm is also plotted to show the agreement [13]. It is observed that for a given channel electric field and input power shorter gate length devices operate at higher temperature and is attributed to the higher power densities in shorter gate length devices due to their lower channel area. At elevated temperatures the effective mobilities for shorter gate length devices are greatly reduced from their room temperature values. To demonstrate the temperature dependence, results are calculated at room temperature and by considering temperature rise due to thermal effects. Due to higher mobility and saturation velocity, calculated output power

at isothermal condition (300K) is higher than that obtained by taking thermal effects into account. The difference is less for 0.75μm gate length device as it operates at the lower temperature. The difference increases with decreasing gate length due to higher operating temperatures. Similar results are obtained for the calculated power gain as shown in Fig.3. Isothermal power gain of the 0.30μm gate length device is 9.5dB. With thermal effects taken into account, the calculated power gain is reduced by 2.25dB. For 0.75μm gate length device the difference is about 0.6dB. On the same figure, the measured data for L = 0.3μm is plotted to show good agreement [13]. Similar results are obtained for power added efficiency (PAE) as shown in Fig.4.

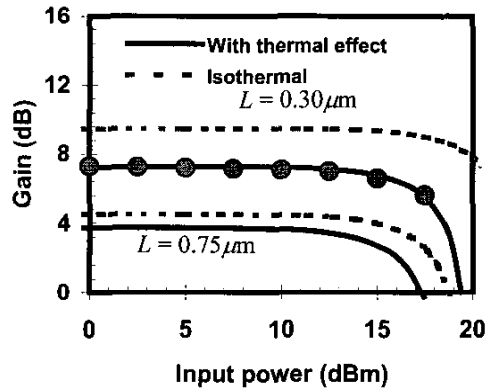

Fig. 3. Variation of power gain as a function of input power for L×100μm GaN MESFET at 2GHz. Measured results are shown by circles for L = 0.3μm [13].

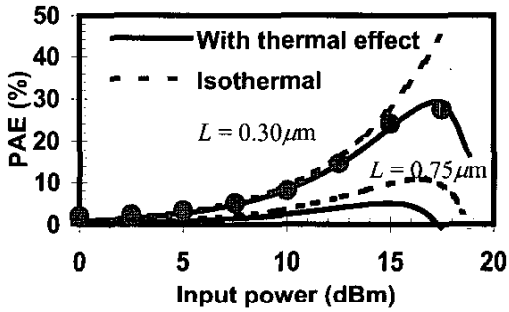

Fig. 4. Variation of PAE as a function of input power for L×100μm GaN MESFET at 2GHz. Measured results are shown by circles for L = 0.3μm [13].

Fig.5 shows the variation of third-order intermodulation (IM3) as a function of output power with gate length as a parameter. Better IM3 is obtained for shorter gate length devices due to reduced nonlinearities resulting from higher transconductance and lower capacitances. At elevated temperatures, transconductance decreases due to lower mobility and saturation velocity and device nonlinearity increases resulting in higher IM3 for a given output power level. At higher output power level nonlinearity increases resulting even higher IM3 due to thermal effects.

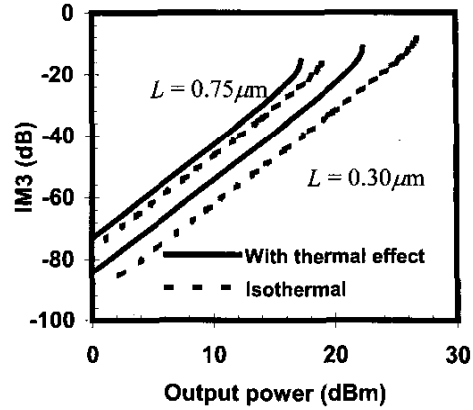

Fig. 5. Variation of IM3 as a function of input power with gate length as parameter at 4GHz.

IV. Conclusion

Short channel devices demonstrated higher output power, power gain and PAE, however, better thermal stability is obtained in long channel devices. Lower IM3 is observed in shorter gate length devices which increase greatly due to self-heating effects.

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